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Measurements of Real ESD Threats Have Been Ignored Too Long

Electrostatic discharge (ESD) protection circuits are built into every pin of an integrated circuit (IC) to protect the core operating circuits. Many different standards groups have assumed the responsibility of producing ESD testing standards for the IC industry. Existing standards are based on measurements of the real ESD threat made 20 years ago with instrumentation we would hardly consider precise today. Circuits designed from that data still form the basis of today's ESD test equipment. In addition, as ICs became larger with more connections to the outside world, the number of pins to be tested increased. The simulated tester waveform was changed to cause minimum distortion to waveforms, which pass through a complex switching matrix to select any pair of pins. The subnanosecond current discharge risetime found in real events was slowed to 2–10 ns risetime to prevent ringing of the test waveform on 200–500 pin IC testers. This and other assumptions made at that time ignored some of the real parameters known to exist in ESD. Standards and reliability groups continue blindly to assume that the standards, written around this basic tester design, provide an acceptable simulation test in qualifying ICs for ESD immunity.

Since the first testers were designed, high-speed measurement instrumentation has improved from 1 GHz to over 6 GHz; waveform records have improved from lines on photographic film to 8-bit digital data, and storage of many data points is now an insignificant consideration. Data records long before the trigger event are now possible. From a measurement perspective, data extraction, storage, statistical analysis, and retrieval are far less tedious and more complete.

Testers built to incomplete specifications in the standards did not always provide the same failure levels when testing IC immunity levels. Minor differences in correlation between testers have been experienced since the beginning. Many theories on the causes have been proposed, but there are no definite answers or solutions because there are many possible causes. Early bipolar protection circuits were very simple and operated at 15 V. They were insensitive to minor differences between testers and were able to qualify ICs quite well. The minor differences in test results, which occurred occasionally in the past, have become major differences in recent years.

An explosive evolution in these protection circuits has occurred, and these complex circuits now use CMOS transistors operating at 3 V moving toward 1 V in the near future. Some of these designs are now sensitive to the missing parameters in ESD while others have become sensitive to test waveform artifacts not in ESD. The evolution of IC core operating circuits has been accompanied by a similar evolution in the ESD protection circuits. Differences in test results will increase as silicon protection circuits and ICs continue to improve.

The quality of ESD testing and their standards have therefore suffered from a lack of measurement updates without an effort for periodic investigations of the real threat from ESD. We have recently made measurements of the real voltage and current ESD threats using high-speed digitizers. Our work was done to determine precise parameters needed to identify accurate simulation test requirements. This data shows significantly different ESD threat parameters than that provided by today's ESD testers. It is the first effort to update basic test requirements. The goal is to decrease or eliminate differences between testers. Human body model (HBM) was the first ESD threat defined and developed into a test. It attempted to simulate the energy in the treat, but failed to identify the tremendous variations of the air spark resistance in a charged finger discharge [1]. We found that the resistance of the air spark discharge event is highly variable. This is radically different from the fixed resistor value of 1500 Ω now used in HBM testing.

The great majority of measurements in ESD testing were done to analyze the testers themselves with little or no thought of what the real threat might be. Extensive reviews and analysis of repeatable pulses from testers themselves is less difficult because the measurements are simple. High-speed measurements of highly variable real HBM air spark discharges are certainly more difficult. However, they provide higher value in identifying the threat to be simulated.

Even though measurements of the real event are more complex and variable, how long should an industry ignore a review of the real threat this industry intends to simulate? How many improvements to the tester and the standard can be made without revisiting or reviewing the original threat? The primary reason we chose to make these studies is because ESD

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designers voiced their concerns over different IC failure levels in ESD testing. They have no guidance on which tester to use when very different results occur. Individually, designers do not have the resources to provide logical explanations on why these different failure levels occur.

Basic designs must use significantly more silicon than is needed to provide the excess protection capabilities. Overprotected ICs, qualified by testing with excessive threats, can still fail in the field from parameters missing in the tests. Tester waveform artifact threats cause unexpected and unexplained failures, which may not occur in real life. The test waveform artifacts that fail good parts, force ESD designers to redesign their circuits to pass the required tests, which contain unspecified, unnecessary, and unknown test parameters.

Our latest measurements of the rate of voltage rise have, for the first time, identified that it rises extremely slowly. This is completely contrary to the expectations and SPICE analysis, which ESD designers have always used in their circuit designs. Many ESD protection circuits turn on when a voltage slightly above the IC operating voltage is reached during an ESD event. This new information is very important in ESD protection design. An ESD voltage, which rises slightly above the operating voltage over a period of milliseconds, is very different from present designs, which expect a nanosecond rate of voltage rise to turn on the protection.

Some protection circuits have timers that turn off some hundreds of nanoseconds after the voltage has reached its trigger amplitude. These circuits have been designed using the long-held expectation that the rising voltage and current are simultaneous. When the ESD voltage across a basically open protection circuit raises some milliseconds before the dangerous current discharge pulse, that protection circuit will turn itself off before the current pulse occurs and the clamp is inactivated. This damages the circuit or core at much lower ESD levels because the timed protection circuit operates on voltage not current.

Our measurements also identified that the real ESD event voltage across an IC can exist for a hundred milliseconds after the current pulse. Having the real threat voltage across the device for a few milliseconds before the current discharge and for a hundred milliseconds or more after the peak current discharge can damage gate oxides in the core. Modern gate oxides are much thinner to provide the necessary gain in reduced operating voltage CMOS circuits. Thin gate oxides are now designed to withstand the ESD voltage for far less time than we find it actually exists. The sensitivity to voltage in the dielectric of a gate oxide is not only a factor of voltage, but of the time that a voltage is across the dielectric.

This new information may have a direct effect on the design of lower voltage CMOS circuits and could put serious limitations on ICs operating at reduced voltages. Present and future dielectrics being designed for gate insulators in these circuits may be at risk. Reliability considerations would suggest that voltages across these thin dielectrics, which last much longer than expected, should be of great interest. This is not the case however, and people in charge of reliability technology have been as unconcerned with these developments as are those in charge of ESD testing technology.

An analysis of our measurements has shown that air spark ESD discharges are extremely nonlinear in resistance over time. The resistance of a spark discharge begins at an extremely high resistance with just a few electrons flowing. The current avalanches and increases to its peak amplitude in a relatively short time. This occurs when the spark resistance reaches its lowest value. After the peak current is reached, the discharge current from the capacitor source begins to decrease. Because the spark resistance is inversely proportional to the current through it, the spark resistance then begins to increase exponentially until the current can no longer sustain the spark discharge of electrons and ions. This can continue for many hundreds of microseconds. If the resistance is plotted on a log scale of resistance versus time, it will form a distorted V or U curve. The spark resistance will start at infinity and decrease toward a minimum resistance of 1 or 2 kΩ when a human finger and a metal conductor are the electrodes. It then increases to infinity at a slower rate.

We are continuing these measurements to clearly define the typical spark resistance throughout its brief life. Because ESD protection circuits can be abruptly nonlinear in their resistance characteristics, both it and the nonlinear resistance conditions of the spark must be well defined. Testing with a known true simulation of the real threat will simplify design efforts by eliminating the unknown variables, which ESD designers must now accept.

Our measurements of the real ESD threats also discovered that the amount of water in the air plays a major factor in the ESD threat level. We found that for any particular voltage, dry air causes the highest current and the highest discharge threats. This is not only due to the decreased amounts of charge that can be stored on a conductor that rapidly leaks off but increased humidity also reduces the spark current amplitudes by increasing the spark resistances during the discharge. The humidity factor was not identified in the measurements of 20 years ago, although that data could have easily been recorded.

Accurate measurements in developing a standard are very important if the standard is to provide controlled and known test conditions. Under testing will quickly be identified because parts will fail in the field. However,

over design and over testing is good for the customer but costly for the manufacturer. It can remain undiscovered for many years if the real threat conditions are not clearly identified. Measurements to determine the real parameters should not have been ignored this long.

Because ESD test or reliability groups control the standards, ESD designers are on the bottom of the ladder. They are also in separate companies and cannot easily communicate to organize and present their concerns on the existing testers and standards. The present tests and standards will continue because organized ESD experts in standards groups are unconcerned with the real threat and can ignore the new data we have measured. In our effort to improve ESD standards during the last two years, we have presented this data for consideration in the standards, but so far we have been unsuccessful. Failures from tester artifacts are difficult to determine by individuals at separate companies, so their circuits are improved without fanfare. Real or false ESD failures are not advertised for obvious reasons, and false qualifications are unknowingly accepted.

How long will this new understanding of the real threat be ignored before standards and reliability groups choose to consider the simulation accuracy as a part of testing standards and tester requirements? How long will it be before over testing and tester artifacts that fail good parts and a lack of testing with the slow voltage rise continue while designers demand a much closer simulation of the real ESD threat? Answers to these questions will depend on the ability to force these issues into consideration.

References

[1] J. Barth, J. Richner, and R. Ashton, "Voltages before and after current in HBM testers and real HBM," in *Proc. ESDA Symp.*, Sept. 2005.

Jon Barth is a Life Member of the IEEE. His experience developed in the manufacture of fast pulse HV instrumentation for government laboratories. With cessation of nuclear weapons testing at the Nevada Test Site, he transferred his time domain technology to ESD test equipment.

my favoriteexperiment *continued from page 59*

mux simply could not discharge fast enough over one or even two sample periods. Another option in this case might have been to rescale the angle sensor and reduce the signal level to a similar millivolt level; unfortunately the dynamic range requirements for angle sensing in this application were huge.

Sometimes using high-channel-count multiplexed A/Ds have drawbacks that cannot be overcome. In these situations, several discrete or semidiscrete A/D chips will be required. High sample speeds combined with high resolution and high impedances usually force such solutions. I am currently working on a redesign of an earlier described project, which now involves capturing true 24-b data consisting of several channels of millivolt level strain-gage data along with critical wide dynamic range angle indications within a rotational environment. Fortunately, several dual channel seismic DAQ chips exist that will allow me to overcome my expected crosstalk problems by carefully mapping my signals into discrete chips. The design will use a dual-channel, multiplexed sigma-delta ($\Sigma - \Delta$) A/D to acquire the high-level angle data and five separate dual-channel, multiplexed $\Sigma - \Delta$ A/D chips dedicated exclusively to various low-level strain data. This combination, along with signal averaging (thanks to our rotating application) and low resistance gauges, should allow the required tens of nanostrain resolution; difficult under any condition.

Next time your design calls for a multichannel analog-digital converter solution, try a simple experiment. During development, when your design is breadboarded or prototyped, connect a function generator to a near-middle channel, say channel number two in a four-channel application. Ground the remaining three channels though a 1 kΩ resistor and then acquire data from all the channels. You will probably see channel two contains your signal, channel three is showing a component of channel two, and channel four has a smaller component of channel two. Depending on the crosstalk mechanism, channel one my also have data of a lesser or greater value than channel four! Crosstalk.

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