The Total CDM Voltage Threat

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Purpose of Study

- After VFTLP has identified the TDDB threat to oxides,
- The total CDM threat to oxides inside the package needs to be identified
- Package capacitance has been thoroughly considered
- Package parasitic lead inductance can now be included in the analysis

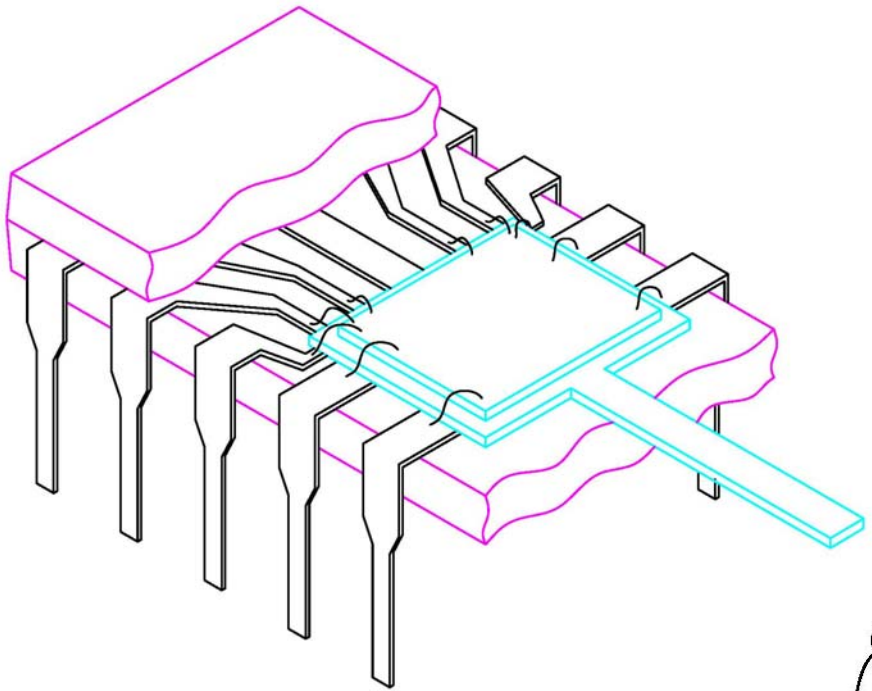
Outline of Study

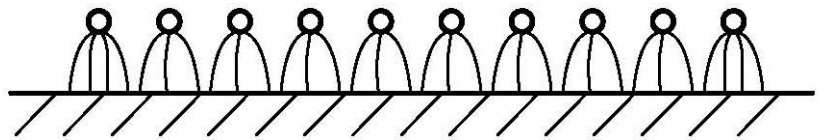
- VFTLP identifies the Initial Voltage Impulse (IVI) for the specific GOX threat
- Package parasitic inductance introduces a previously unidentified voltage threat
- It creates the Secondary Voltage Impulse (SVI); which hasn’t been analyzed
- Both circuit and package elements must be considered
- For complete analysis of the GOX voltage threat

Including All Package Parasitics in CDM threat analysis

- Until now all package parasitics have been combined to form a simple LRC circuit
- This simulates the CDM waveform
- But eliminates a detailed analysis of individual parasitics
- CDM has included package capacitance but not the package lead inductance

Multiple leads combine E field for primary package capacitance





Multiple Wires Above a Ground Plane

Package Parasitics

- Total CDM Capacitance is 10-20% from Die alone
- 80-90% of total Package capacitance is from package leads
- The one lead carrying the discharge current is a high impedance transmission line considered here as an inductance
- VFTLP measures package inductance as a specific and separate parameter

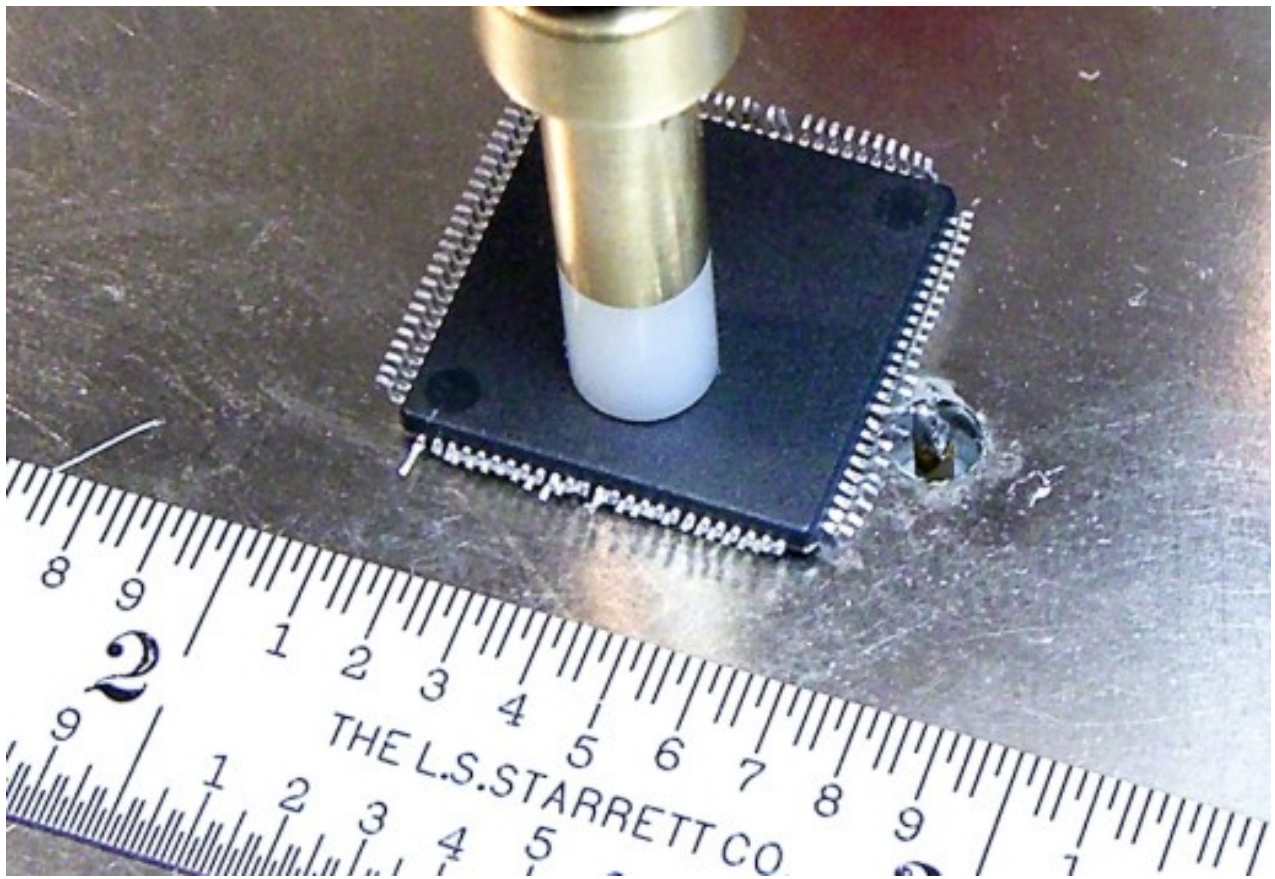
Package Inductance is a Separate Parameter, as is Package Capacitance

- To identify voltages inside the package the discharge current path must be considered separately
- We must know the parasitic inductance the current flows through, viewed from inside the package

Xilinx XC9572 100 pin QFP

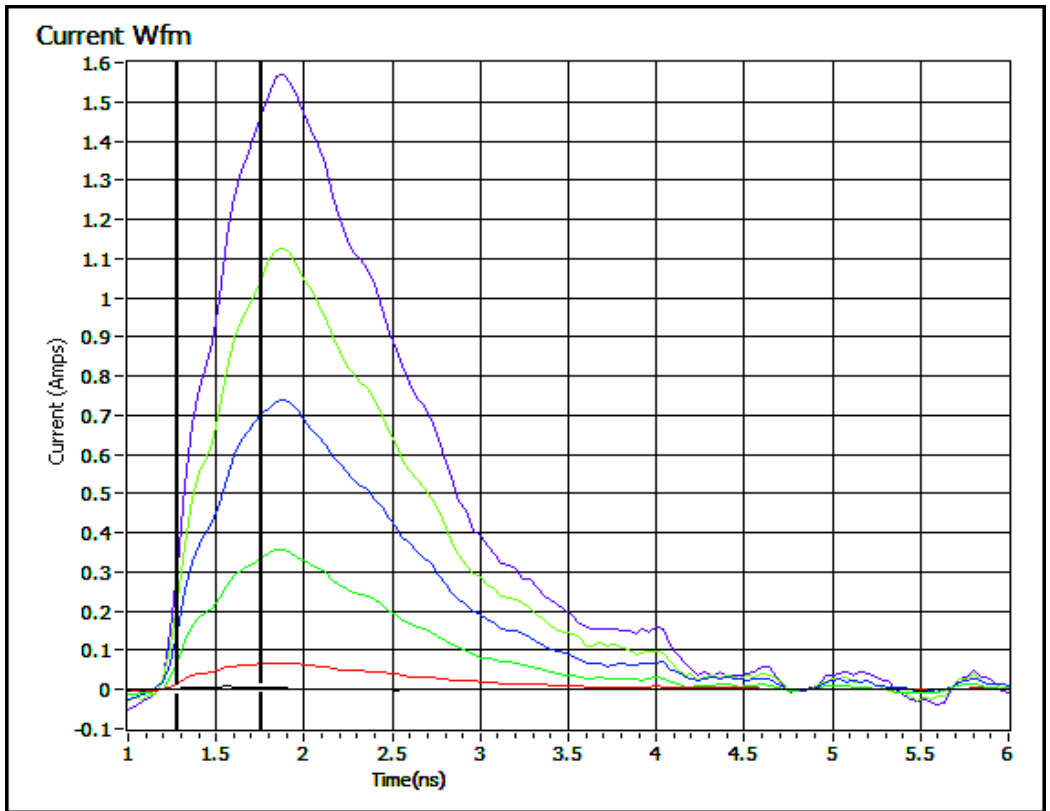
- CC-VFTLP Center pin Measurement of current

  risetime



Current Risetime Measured With 100 ps VFTLP Test Pulse

- Xilinx XC9572 100 pin QFP
- 480 ps current risetime

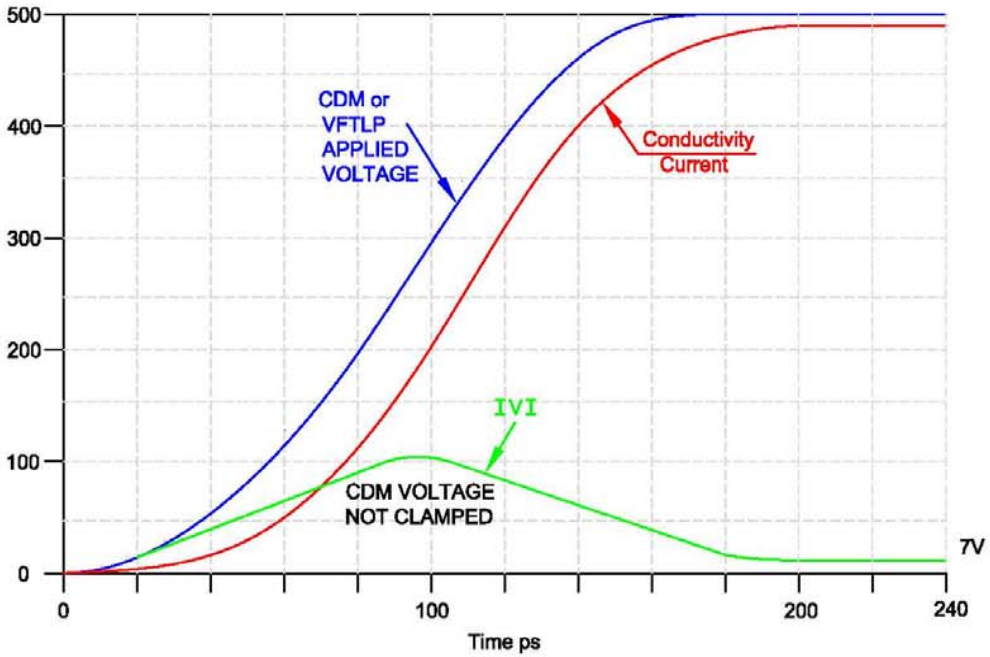


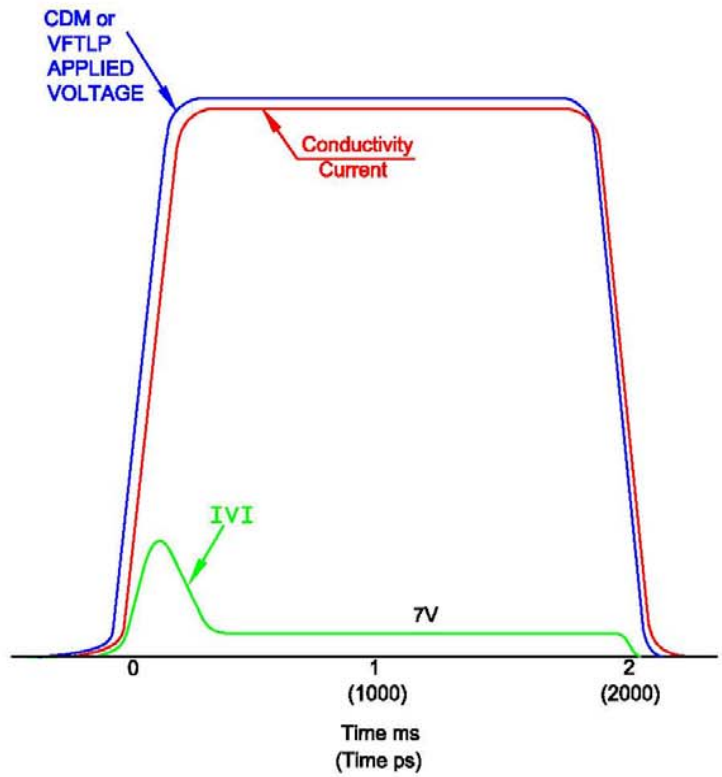
Reverse Polarity is Generated by the Package Lead Inductance

- 1 Amp CDM source at 100 ps circuit constants into a 15 nH package lead can produce 70 volts at a 480 ps risetime
- This opposite CDM polarity voltage will be applied to the Reverse protection CDM element.
- It will respond with its own IVI voltage not immediately clamped because of the diode turn-on time

Voltage Generated by silicon clamp time delay

- Two time domain plots show the Initial Voltage Impulse (IVI)

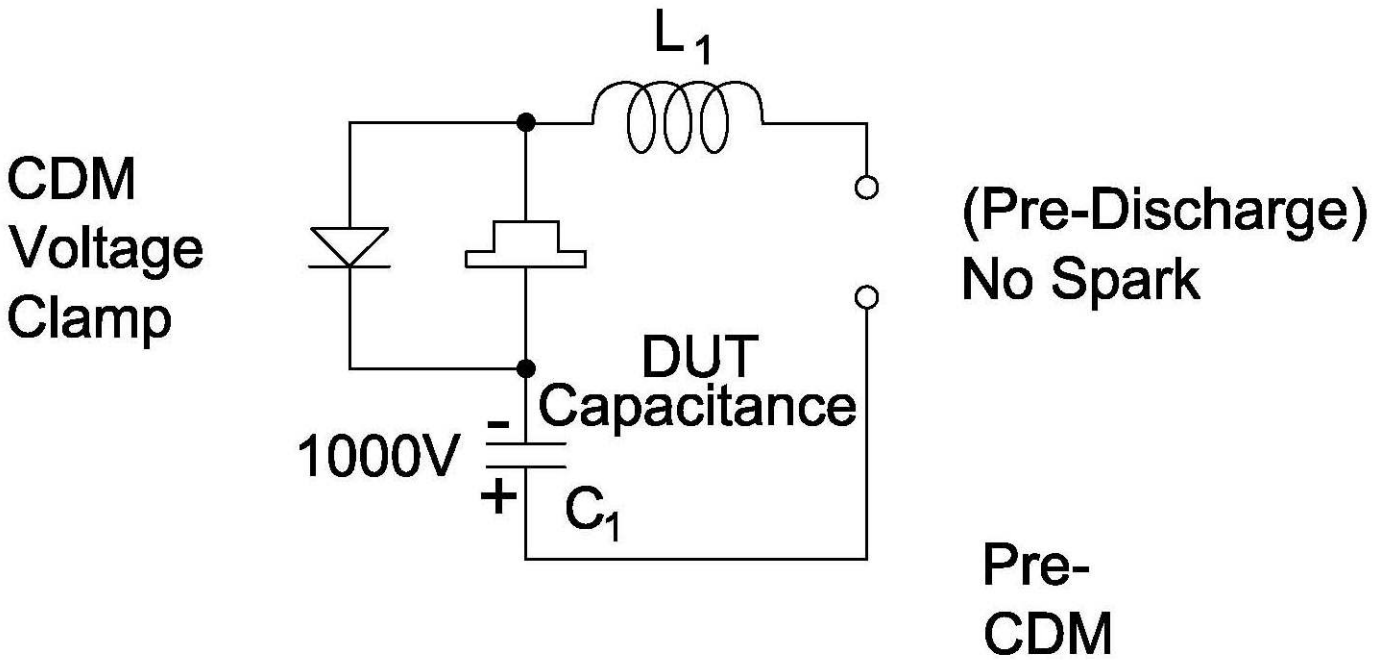




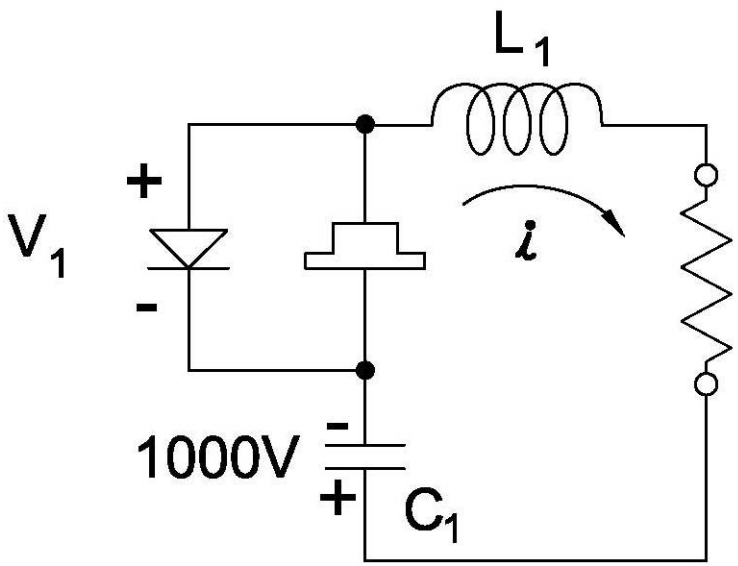
Both Forward and Reverse ESD voltage clamps create their own IVI

- Snapback or diode protection clamps produce their own IVI
- The Reverse protection diode also produces its own IVI
- Each is measurable with VFTLP

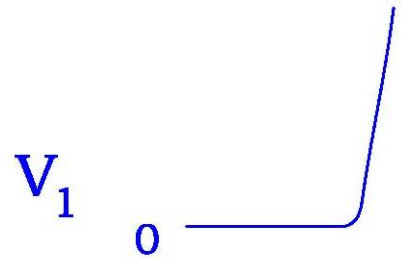
The lead Inductance generates a different voltages inside the package



As CDM voltage increases

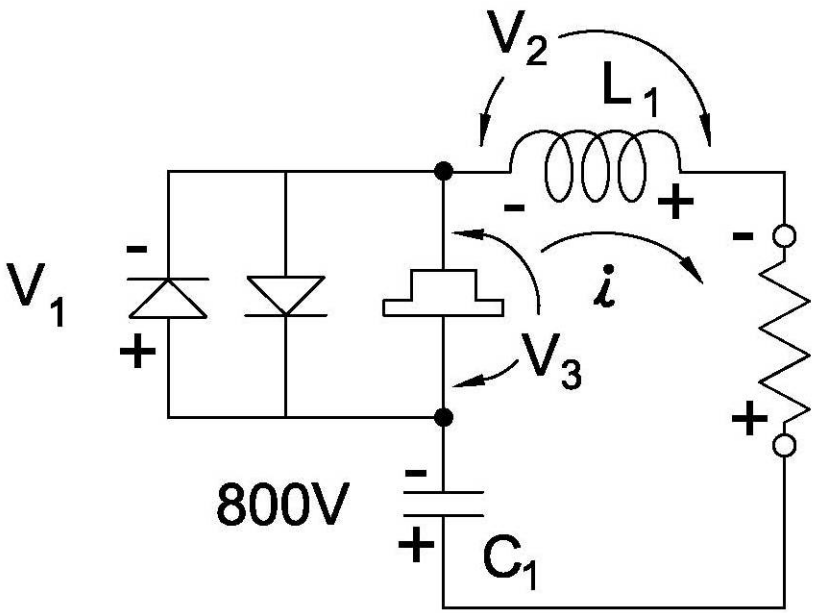


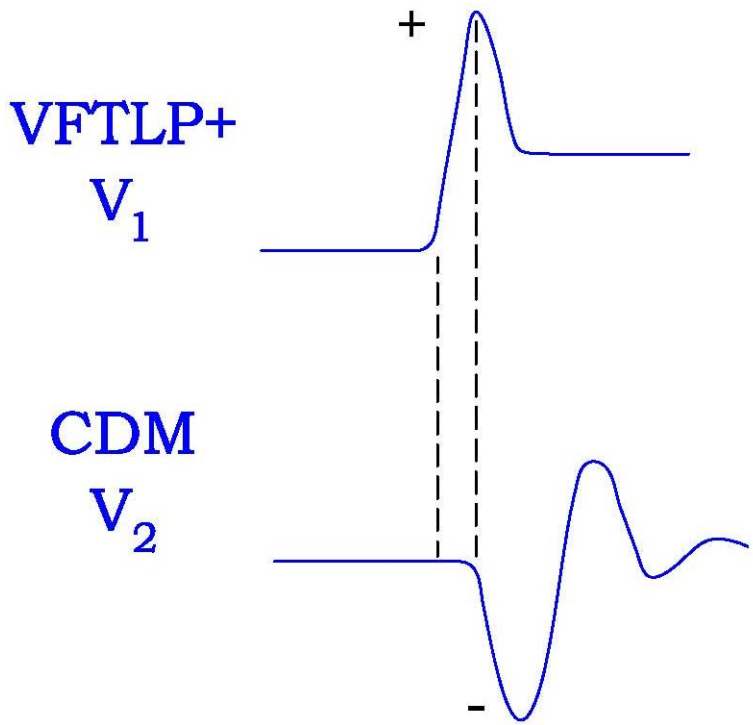
Spark Initiates (High R)



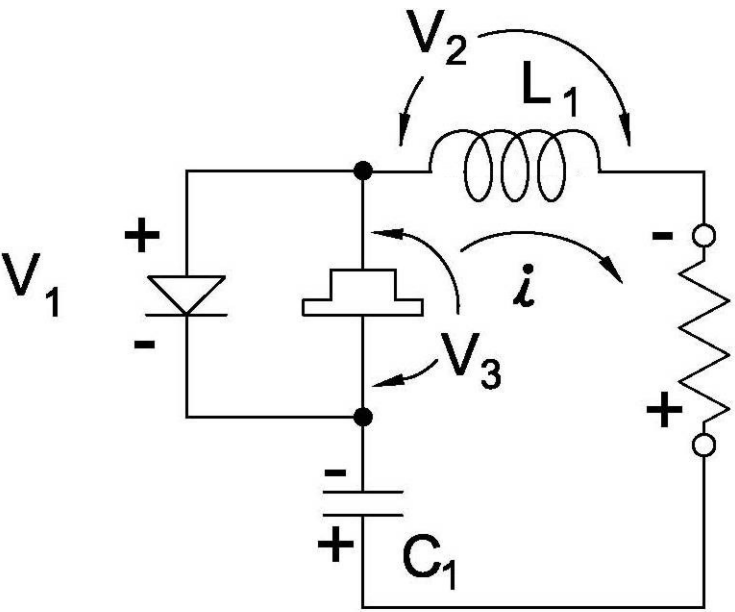
Discharge Begins

CDM or VFTLP Voltage increases to its maximum



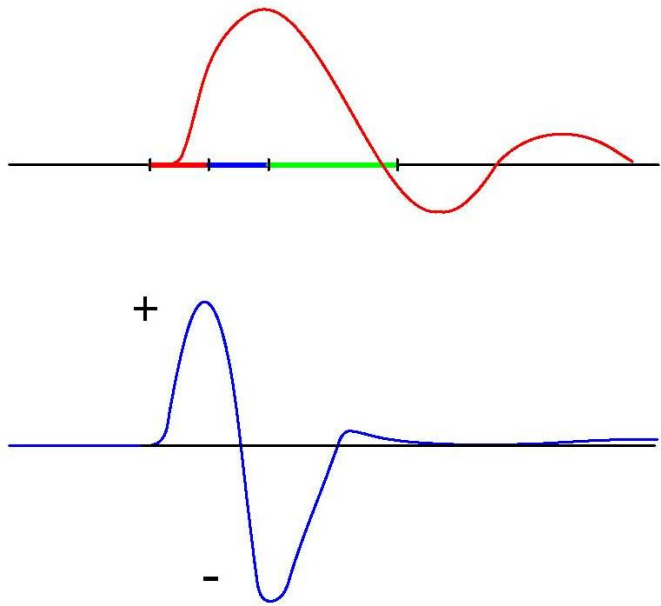


At the End of CDM Discharge the Threat Voltage Could be Complex



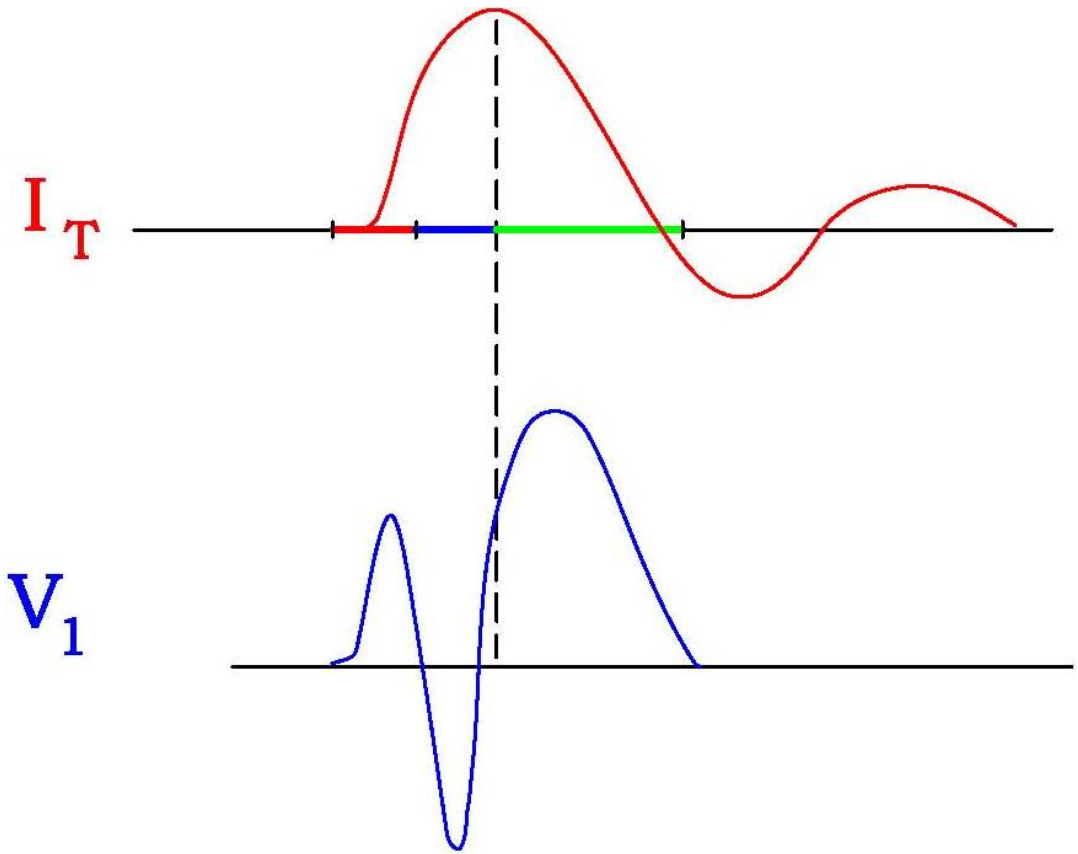
Spark Resistance

End of CDM Discharge



Extreme voltage swings may be possible

- Timing of IVI and current through inductance can create complex voltages



Rapid Voltage Reversals in Oxides May Create an Additional Threat

- Voltage reversals in highly stressed dielectrics greatly shortens its life
- Voltage reversals in gate oxide dielectrics have to be studied to determine any extra TDDB threat

Conclusion

- Presentation of a new oxide voltage threat has been proposed using VFTLP data
- Its bipolar amplitude and width depend on:
  - Turn-on time delay of silicon Forward & Reverse protection elements
  - Package lead parasitic inductance
  - Circuit element parameters
- Further analysis is needed to accurately identify voltage amplitude, reversal, and width
- High Speed VFTLP provides this data analysis opportunity